Ordering number: EN 4303B

CMOS LSI

SANYO No.4303B

LC866132A, 866128A, 866124A

8-Bit Single Chip Microcomputer

LC866132A On-chip 32K-Byte ROM and On-chip 640-Byte RAM 8-Bit Single Chip Microcomputer
LC866128A On-chip 28K-Byte ROM and On-chip 640-Byte RAM 8-Bit Single Chip Microcomputer
LC866124A On-chip 24K-Byte ROM and On-chip 640-Byte RAM 8-Bit Single Chip Microcomputer

Overview

The LC866132A/28A/24A microcomputers are 8-bit single chip microcomputers with the following on-chip functional blocks :

- CPU : Operable at a minimum bus cycle time of 0.5μs (microseconds)
- On-chip ROM Maximum Capacity : 32K bytes
- On-chip RAM Capacity : 640 bytes
- VFD automatic display controller/drivers
- 16-bit timer/counter (or two 8-bit timers)
- 16-bit timer/PWM (or two 8-bit timers)
- Eight-channel 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits
- 14-source 10-vectored interrupt system

All of the above functions are incorporated on a single chip.

Features

(1) Read-Only Memory (ROM) :
- LC866132A 32512 x 8 bits
- LC866128A 28672 x 8 bits
- LC866124A 24576 x 8 bits

(2) Random Access Memory (RAM) : 640 x 8 bits

(3) Minimum bus cycle time : 0.5μs (using 12MHz CF resonator oscillation)
Bus cycle time means ROM-read period.

(4) Minimum instruction cycle time : 1μs (using 12MHz CF resonator oscillation)
The LC866132A/28A/24A is constructed to read ROM twice within one instruction cycle. The performance capability of the LC866132A/28A/24A is about 1.7 times that of our 4-bit microcomputers, the LC66000 series.

Bus cycle time	Cycle time	System clock oscillation	Frequency	Supply
0.5μs	1μs	ceramic (CF) oscillation	12MHz	4.5 to 6.0V
2μs	4μs	ceramic (CF) oscillation	3MHz	2.5 to 6.0V
7.5μs	15μs	Internal RC oscillation	800kHz	2.5 to 6.0V
183μs	366μs	Crystal (X'tal) oscillation	32.768kHz	2.5 to 6.0V

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(5) Ports :

- Input/output ports	:	3 ports (24 terminals)
- Input/output port programmable in nibble units	:	1 port (8 terminals)
- Input/output port programmable in a bit	:	2 ports (16 terminals)
- Input ports	:	2 ports (13 terminals)
- VFD output ports	:	32 terminals
- Large current output for digit	:	16 terminals

- Pull-down resistor option available

(6) VFD automatic display controller

- Segment/digit output pattern programmable
  Any segment/digit combination available
  VFD parallel-drive available
- 16-step dimmer function available

(7) AD converter

- Eight-channel 8-bit AD converter

(8) Serial-interfaces

- Two 8-bit serial-interface circuits (LSB first/MSB first function available)
- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(9) 8-bit PWM outputs

- Output terminal for only PWM
- Static output available

(10) Timers

- Timer 0
  16-bit timer/counter
  2-bit prescaler + 8-bit programmable prescaler
  Mode 0 : Two 8-bit timers with programmable prescaler
  Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter
  Mode 2 : 16-bit timer with programmable prescaler
  Mode 3 : 16-bit counter
  The resolution of Timer0 is 1 t_{CYC}, the cycle time.
- Timer 1
  16-bit timer/PWM
  Mode 0 : Two 8-bit timers
  Mode 1 : 8-bit timer + 8-bit PWM
  Mode 2 : 16-bit timer
  Mode 3 : Variable-bit PWM (9 to 16 bits)
  In Mode 0/1, the resolution of Timer1/ PWM is 1 t_{CYC}.
  In Mode 2/3, the resolution is selectable; t_{CYC} or 1/2 t_{CYC} by program.
- Base timer
  Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock).
  Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock).
  The Base timer clock selectable; 32.768kHz crystal oscillation, System clock, and Programmable prescaler output of Timer 0.

(11) Buzzer output

- The Buzzer sound frequency selectable; 4KHz, 2KHz (using 32.768kHz crystal oscillation for base timer clock)

(12) Remote-control receiver (using P73/INT3/T0IN terminal)

- Noise rejection available
- The interrupt polarity selectable

(13) Watchdog timer
- The watchdog timer requires a resistor R and a capacitor C.
- Operation selectable : interrupt or reset

(14) Interrupt system
- 14-source 10-vectored interrupts :
  1. External interrupt INT0
  2. External interrupt INT1
  3. External interrupt INT2, timer/counter T0L (lower 8 bits)
  4. External interrupt INT3, base timer
  5. Timer/counter T0H (upper 8 bits)
  6. Timer T1L, timer T1H
  7. Serial-interface SIO0
  8. Serial-interface SIO1
  9. AD converter
  10. VFD display controller, port 0
- Interrupt Priority control available

  Interrupt Priority control register is included.

  These microcomputers allows 3-level interrupt ; low-, high- and highest-level of the multiplex interrupt. It can sepcify a low- or high-level interrupt priority from INT2/T0L through VFD display controller/port 0, the above interrupt number from 3 to 10. It can also specify a low- or the highest-level interrupt priority to INT0 and INT1.

(15) Real-time service operation

The Real-Time Service (RTS) functions the data-transfer between the Special Function Registers at acknowledging the interrupt request. The RTS starts within 1 cycle-time and completes within 5 cycle-times after occurring the interrupt request.

(16) Sub-routine stack levels
- 128 levels maximum (Set the stack inside a RAM)

(17) Multiplication and division

16 bits × 8 bits (7 instruction cycle-times)

16 bits / 8 bits (7 instruction cycle-times)

(18) Three oscillation circuits
- On-chip RC oscillation circuit using for the system clock
- On-chip CF oscillation circuit using for the system clock
- On-chip crystal oscillation circuit using for the system clock and for time-base clock

  The XT1 terminal can be used as $\overline{P74}$.

(19) Standby function

-HALT mode function

The HALT mode is used for reducing the power dissipation. In this mode, the program execution is stopped. This mode can be released by the interrupt request signals or the system reset.

-HOLD mode function

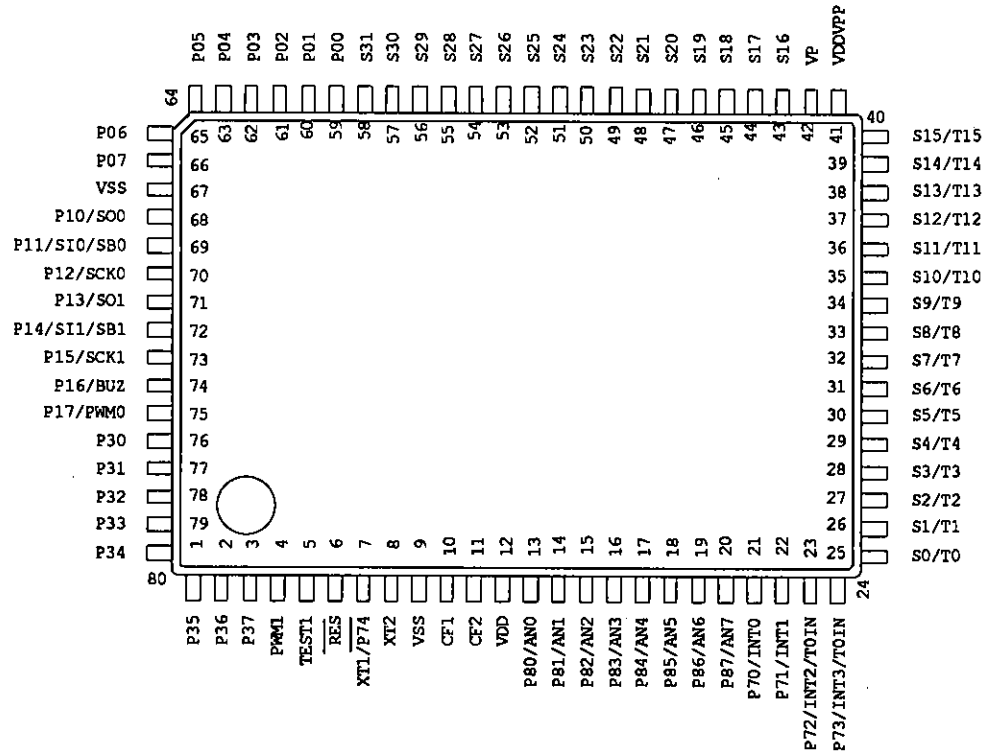
- Reset terminal ($\overline{RES}$) is set to Low level.
- One of two terminals, P70/INT0/T0IN and P71/INT1/T0IN, is set to the assigned level (programmable).
- Port 0 agrees the specified conditions.

(20) Factory shipment
QFP80E delivery form

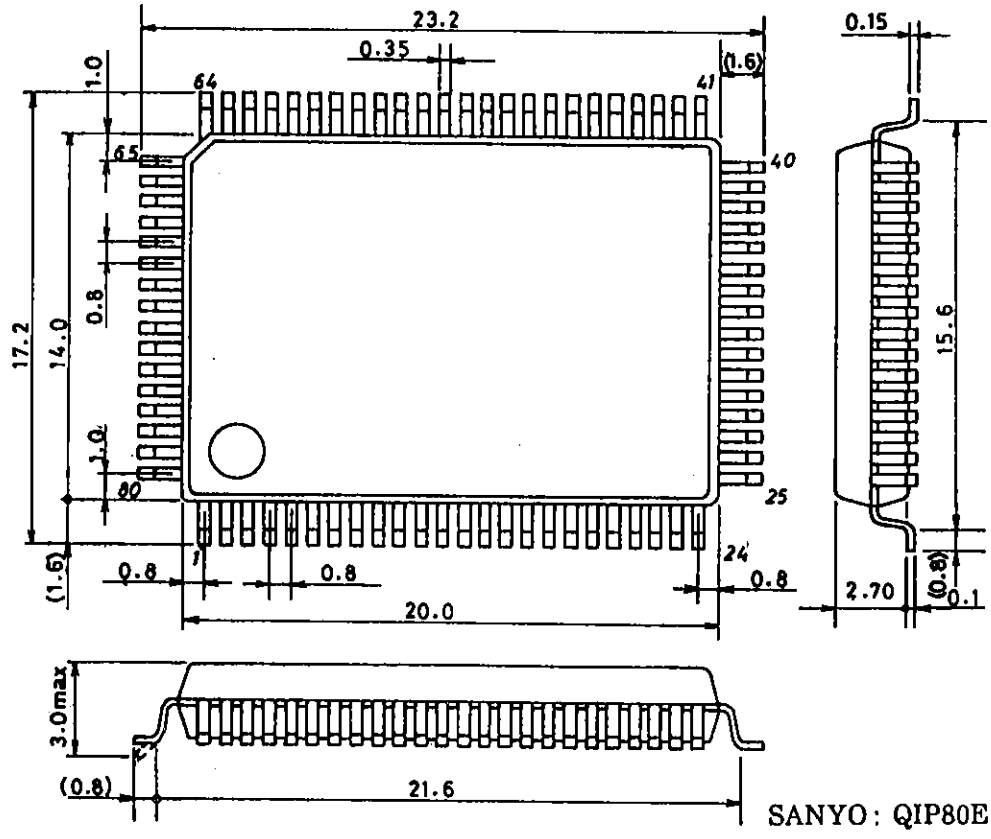
(21) Development support tools

Evaluation (EVA) chip	:	LC866098
EPROM version	:	LC86E6132
One-time version	:	LC86P6132
Emulator	:	EVA-86000 + ECB866000 (Evaluation chip board) + POD866100 (POD)

Pin Assignment

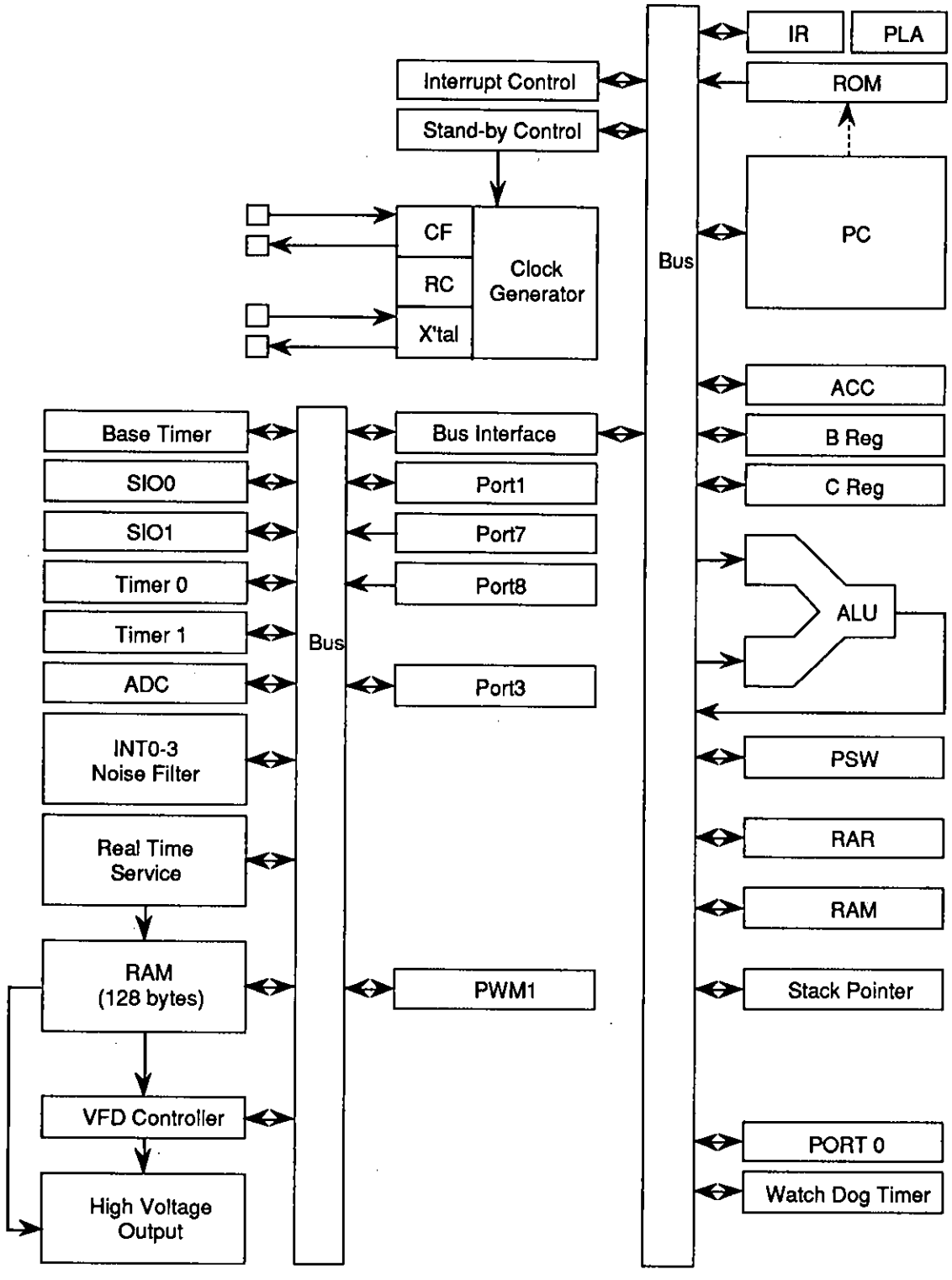


Package Dimensions 3174
(unit: mm)



SANYO: QIP80E

System Block Diagram



Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS</td><td></td><td>Power pin(-)</td><td></td></tr>
<tr><td>VDD</td><td></td><td>Power pin(+)</td><td></td></tr>
<tr><td>VP</td><td></td><td>Power pin(-) for VFD output pull-down resistor</td><td></td></tr>
<tr><td>VDDVPP</td><td></td><td>Power pin(+) *1</td><td></td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>•8-bit input/output port
•Input for port 0 interrupt
•Input/output in nibble units
•Input for HOLD release</td><td>•Pull-up resistor :
Provided/ Not provided
•Output form :
CMOS/N-channel open drain</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in a bit unit.
•Other pin functions
P10 : SIO0 data output
P11 : SIO0 data input/ bus input/output
P12 : SIO0 clock input/output
P13 : SIO1 data output
P14 : SIO1 data input/ bus input/output
P15 : SIO1 clock input/output
P16 : Buzzer output
P17 : Timer 1 output (PWM output)</td><td>Output form :
CMOS/N-channel open drain</td></tr>
<tr><td>PORT3
P30 to P37</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in bit unit.</td><td>•Pull-up resistor :
Provided/ Not provided
•Output form :
CMOS/N-channel open drain</td></tr>
<tr><td>PORT7
P70
P71 to $\overline{P74}$</td><td>
I/O
I</td><td>•5-bit input port
•Other pin functions
P70 : INT0 input/HOLD release /N-channel Tr. output for watchdog timer
P71 : INT 1 input/HOLD release
P72 : INT 2 input/timer 0 event input
P73 : INT 3 input with noise filter/timer 0 event input
$\overline{P74}$: Input terminal XT1 for 32.768kHz crystal oscillation
•Interrupt received form, vector addresses
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>High level</th><th>Low level</th><th>Vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>Pull-up resistor :
Provided/ Not provided
(P70,71,72,73)
* $\overline{P74}$ has no pull-up resistor option.</td></tr>
<tr><td>PORT8
P80 to P87</td><td>I</td><td>•8-bit input port
•Other functions
AD input port (8 port pins)</td><td></td></tr>
<tr><td>PWM1</td><td>O</td><td>Output terminal for only 8-bit PWM (CMOS output)</td><td></td></tr>
</table>

Pin name	I/O	Function description	Option
S0/T0 to S6/T6	O	Output for VFD display controller segment/timing in common	Pull-down resistor : Provided/ Not provided
S7/T7 to S15/T15	O	Output for VFD display controller segment/timing with internal pull-down resistor in common	
S16 to S31	O	Output for VFD display controller segment	Pull-down resistor : Provided/ Not provided.
$\overline{RES}$	I	Reset pin	
TEST1	O	Test pin Should be left unconnected. Output fixed high	
XT1/$\overline{P74}$	I	•Input pin for 32.768kHz crystal oscillation. •Other function Input port $\overline{P74}$ In case of non use, connect to VDD.	
XT2	O	Output pin for 32.768kHz crystal oscillation. In case of non use, should be left unconnected.	
CF1	I	Input pin for ceramic resonator oscillation	
CF2	O	Output pin for ceramic resonator oscillation	

* All of port options can be specified in bit unit.

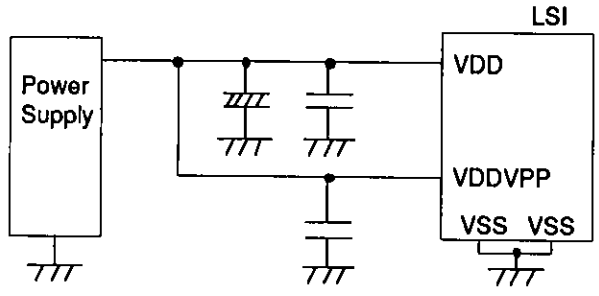
* A state of pins at reset.

Pin name	Input/output mode	A state of pull-up resistor specified at the pull-up option
Port 0 Ports 70, 71, 72, 73	Input	Fixed pull-up resistor exist
Ports 1, 3	Input	Programmable pull-up resistor OFF

Pin name	A state of P-channel transistor
S0/T0 to S15/T15	P-channel transistor OFF
S16 to S31	P-channel transistor OFF

Notes • Short-circuit the VDD terminal to the VDDVPP terminal.
• Two of VSS terminals must be short-circuited each other.

*1 Connect like the following figure to reduce noise into a VDD terminal.



1. Absolute maximum ratings / VSS = 0 V and Ta = 25°C

Parameter		Symbol	Pins	Conditions	Limits				
					VDD[v]	min.	typ.	max.	unit
Supply voltage		VDDMAX	VDD,VDDVPP	VDD=VDDVPP		-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71, 72, 73, $\overline{74}$ •Port 8 •$\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-45		VDD+0.3	
Output voltage		VO(1)	•S0/T0 to S15/T15 •S16 to S31			VDD-45		VDD+0.3	
		VO(2)	PWM1			-0.3		VDD+0.3	
Input/output voltage		VIO	•Ports 0, 1, 3 •Port 70			-0.3		VDD+0.3	
High Level output current	Peak output current	IOPH(1)	•Ports 0, 1, 3 •PWM1	•CMOS output •At each pins		-4			mA
		IOPH(2)	S0/T0 to S15/T15	At each pins		-30			
		IOPH(3)	S16 to S31	At each pins		-15			
	Total output current	ΣIOAH(1)	•Ports 0, 1, 3 •PWM1	The total all pins		-30			
		ΣIOAH(2)	•S0/T0 to S15/T15 •S16 to S31	The total all pins		-140			
Low Level output current	Peak output current	IOPL(1)	•Ports 0, 1, 3 •PWM1	At each pins				20	
		IOPL(2)	Port 70	At each pins				15	
	Total output current	ΣIOAL(1)	Port 0	The total all pins				40	
		ΣIOAL(2)	Port 1	The total all pins				40	
		ΣIOAL(3)	•Port 3 •PWM1	The total all pins				40	
Power dissipation		Pdmax	QFP80E	Ta=-30°C to +70°C				480	mW
Operating temperature range		Topg				-30		70	°C
Storage temperature range		Tstg				-65		150	

2. Recommended operating range / Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Limits			
			VDD[v]	min.	typ.	max.	unit
Operating supply voltage range	VDD(1)	VDD	0.98μs ≦ tCYC ≦ 400μs	4.5		6.0	V
	VDD(2)		3.9μs ≦ tCYC ≦ 400μs	2.5		6.0	
HOLD voltage	VHD	VDD	RAMs and Registers hold voltage at HOLD mode.	2.0		6.0	
Pull-down voltage	VP	VP		2.5 to 6.0	-35		VDD
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	2.5 to 6.0	0.4VDD +0.9		VDD
	VIH(2)	•Ports 1, 3 •Ports 72, 73 (Schmitt)	Output disable	2.5 to 6.0	0.75VDD		VDD
	VIH(3)	•Port 70 port input/ interrupt •Port 71 •$\overline{RES}$ (Schmitt)	Output N-channel Tr. OFF	2.5 to 6.0	0.75VDD		VDD
	VIH(4)	Port 70 Watchdog timer input	Output N-channel Tr. OFF	2.5 to 6.0	0.9VDD		VDD
	VIH(5)	•Port $\overline{74}$ •Port 8		2.5 to 6.0	0.75VDD		VDD
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	2.5 to 6.0	VSS		0.2VDD
	VIL(2)	•Ports 1, 3 •Ports 72, 73 (Schmitt)	Output disable	2.5 to 6.0	VSS		0.25VDD
	VIL(3)	•Port 70 Port input/ interrupt •Port 71 •$\overline{RES}$ (Schmitt)	Output N-channel Tr. OFF	2.5 to 6.0	VSS		0.25VDD
	VIL(4)	Port 70 Watchdog timer input	Output N-channel Tr. OFF	2.5 to 6.0	VSS		0.8VDD -1.0
	VIL(5)	•Port $\overline{74}$ •Port 8		2.5 to 6.0	VSS		0.25VDD
Operation cycle time	tCYC			4.5 to 6.0	0.98		400 μs
				2.5 to 6.0	3.9		400

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	11.76	12	12.24	MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	2.5 to 6.0	2.94	3	3.06	
	FmRC		RC oscillation	2.5 to 6.0	0.4	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	2.5 to 6.0		32.768		kHz
Oscillation stable time period (Note 1)	tmsCF(1)	CF1, CF2	•12MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.02	0.2	ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.1	1	
				2.5 to 6.0		0.1	3	
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 to 6.0		1	1.5	s
				2.5 to 6.0		1	3	

(Note 1) The oscillation constant is shown on table1 and 2.

3. Electrical characteristics / Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions		Limits			
				VDD[v]	min.	typ.	max.	unit
Input high current	IIH(1)	•Ports 1, 3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN = VDD (including off-leak current of output Tr.)	2.5 to 6.0			1	µA
	IIH(2)	•Ports 70,71,72, 73 without pull-up MOS Tr. •Potr 8	VIN = VDD	2.5 to 6.0			1	
	IIH(3)	•$\overline{\text{RES}}$	VIN = VDD	2.5 to 6.0			1	
Input low current	IIL(1)	•Ports 1, 3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. VIN = VSS (including off-leak current of output Tr.)	2.5 to 6.0	-1			
	IIL(2)	•Ports 70,71,72, 73 without pull-up MOS Tr. •Port 8	VIN = VSS	2.5 to 6.0	-1			
	IIL(3)	$\overline{\text{RES}}$	VIN = VSS	2.5 to 6.0	-1			
Output high voltage	VOH(1)	•CMOS output of ports 0, 1, 3 •PWM1	IOH = -1.0mA	4.5 to 6.0	VDD - 1			V
	VOH(2)		IOH = -0.1mA	2.5 to 6.0	VDD-0.5			
	VOH(3)	S0/T0 to S15/T15	IOH = -20mA	4.5 to 6.0	VDD-1.8			
	VOH(4)		•IOH = -1.0mA •The current of any unmeasure-ment pin is not over 1 mA.	2.5 to 6.0	VDD - 1			
	VOH(5)	S16 to S31	IOH = -5mA	4.5 to 6.0	VDD-1.8			
	VOH(6)		•IOH = -1.0mA •The current of any unmeasure-ment pin is not over 1 mA.	2.5 to 6.0	VDD - 1			

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[v]	min.	typ.	max.	unit
Output low voltage	VOL(1)	•Ports 0,1,3	IOL = 10mA	4.5 to 6.0			1.5	V
	VOL(2)	•PWM1	IOL = 1.6mA	4.5 to 6.0			0.4	
	VOL(3)		•IOL = 1mA •The current of any unmeasurement pin is not over 1 mA.	2.5 to 6.0			0.4	
	VOL(4)	Port 70	IOL = 1mA	4.5 to 6.0			0.4	
	VOL(5)		IOL = 0.5mA	2.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0, 1, 3 •Ports 70,71,72, 73	VOH = 0.9 VDD	4.5 to 6.0	15	40	70	kΩ
				2.5 to 4.5	25	70	150	
Output off-leakage current	IOFF(1)	•S0/T0 to S6/T6 •S16 to S31 (Without pull-down resistor)	•Output P-channel Tr . OFF •VOUT = VSS	2.5 to 6.0	-1			µA
	IOFF(2)		•Output P-channel Tr. OFF. •VOUT = VDD-40V	2.5 to 6.0	-30			
Pull-down transistor resistor	Rpd	•S0/T0 to S15/T15 •S16 to S31 (With pull-down resistor)	•Output P-channel Tr. OFF •VOUT = 3V •Vp = -30V	5.0	60	100	200	kΩ
Hysteresis voltage	VHIS	•Ports 0, 1, 3 •Ports 70,71,72, 73 •$\overline{RES}$	Output disable	2.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f = 1MHz •Unmeasurement terminals for input are set to VSS level. •Ta = 25°C	2.5 to 6.0		10		pF

4. Serial input/output characteristics / Ta = -30°C to +70°C, VSS = 0 V

Parameter			Symbol	Pins	Conditions	Limits				
						VDD[v]	min.	typ.	max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5	2.5 to 6.0	2			tCYC
		Low level pulse width	tCKL(1)			2.5 to 6.0	1			
		High level pulse width	tCKH(1)			2.5 to 6.0	1			
	Output clock	Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up resistor (1kΩ) when open drain output. •Refer to figure 5	2.5 to 6.0	2			
		Low level pulse width	tCKL(2)			2.5 to 6.0		1/2tCKCY		
		High level pulse width	tCKH(2)			2.5 to 6.0		1/2tCKCY		
Serial input	Data set up time		tICK	•SI0, SI1 •SB0, SB1	•Data set-up to SCK0,1	4.5 to 6.0	0.1			µs
						2.5 to 6.0	0.4			
	Data hold time		tCKI		•Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0	0.1			
						2.5 to 6.0	0.4			
Serial output	Output delay time (Serial clock is extrnal clock)		tCKO(1)	•SO0, SO1 •SB0, SB1	•Use pull-up resistor (1kΩ) when open drain output.	4.5 to 6.0			7/12tCYC +0.2	
						2.5 to 6.0			7/12tCYC +1	
	Output delay time (Serial clock is internal clock)		tCKO(2)		•Data hold from SCK0, 1 •Refer to figure 5	4.5 to 6.0			1/3tCYC +0.2	
						2.5 to 6.0			1/3tCYC +1	

5. Pulse input conditions / Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[v]	min.	typ.	max.	unit
High/Low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	•INT3/T0IN (The noise rejection clock select to 1/1.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	2			
	tPIH(3) tPIL(3)	•INT3/T0IN (The noise rejection clock select to 1/16.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	32			
	tPIL(4)	•$\overline{RES}$	Reset acceptable	2.5 to 6.0	200			μs

6. A/D converter characteristics / Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	Limits				
				VDD[v]	min.	typ.	max.	unit
Resolution	N			4.5 to 6.0		8		bit
Absolute precision	ET		(Note 2)	4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16×tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time = 32×tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 to AN7		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN = VDD	4.5 to 6.0			1	μA
	IAINL		VAIN = VSS	4.5 to 6.0	-1			

(Note 2) The absolute precision excepts the quantization error (±1/2 LSB).

(Note 3) The conversion time means the time to set the complete digital conversion value to the register from the execution of instruction to start conversion.

7.Current dissipation characteristics / Ta = -30°C to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	VDD[v]	Limits min.	typ.	max.	unit
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	•FmCF = 12MHz Ceramic resonator oscillation. •FsXtal=32.768kHz crystal oscillation. •System clock : CF oscillation. •Internal RC oscillation stops.	4.5 to 6.0		10	20	mA
	IDDOP(2)		•FmCF = 3MHz Ceramic resonator oscillation. •FsXtal=32.768 kHz crystal oscillation. •System clock : CF oscillation •Internal RC oscillation stops.	4.5 to 6.0		3	11	
	IDDOP(3)			2.5 to 4.5		1.5	6	
	IDDOP(4)		•FmCF = 0Hz (when oscillation stops). •FsXtal=32.768 kHz crystal oscillation •System clock : RC oscillation	4.5 to 6.0		0.7	2.3	
	IDDOP(5)			2.5 to 4.5		0.4	1.6	
	IDDOP(6)		•FmCF = 0Hz (when oscillation stops). •FsXtal=32.768 kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops.	4.5 to 6.0		35	130	µA
	IDDOP(7)			2.5 to 4.5		15	70	

Parameter	Symbol	Pins	Conditions	VDD[v]	Limits min.	typ.	max.	unit
Current dissipation HALT mode (Note 4)	IDDHALT(1)	VDD	•HALT mode •FmCF = 12MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops.	4.5 to 6.0		5	11	mA
	IDDHALT(2)		•HALT mode FmCF = 3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops.	4.5 to 6.0		2.2	9	
	IDDHALT(3)			2.5 to 4.5		0.8	5	
	IDDHALT(4)		•HALT mode FmCF = 0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	4.5 to 6.0		400	1100	μA
	IDDHALT(5)			2.5 to 4.5		200	700	
	IDDHALT(6)		•HALT mode FmCF = 0Hz (when oscillation stops). •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops.	4.5 to 6.0		25	100	
	IDDHALT(7)			2.5 to 4.5		8	55	
Current dissipation HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5 to 6.0		0.05	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

Table 1 Ceramic resonator oscillation guaranteed constant (main-clock)

A kind of oscillation	Producer	Oscillator	C1	C2
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33pF	33pF
3MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 require K rank (±10%) and SL characteristics.

Table 2 Crystal oscillation guaranteed constant (sub-clock)

A kind of oscillation	Producer	Oscillator	C3	C4
32.768kHz crystal oscillation	Dai Sinku	DT-38(1TA252E00)	18pF	18pF
	Kyocera	KF-38G-13P0200	18pF	18pF

* Both C3 and C4 require J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
•If you use other oscillators herein, we provide no guarantee for the characteristics.

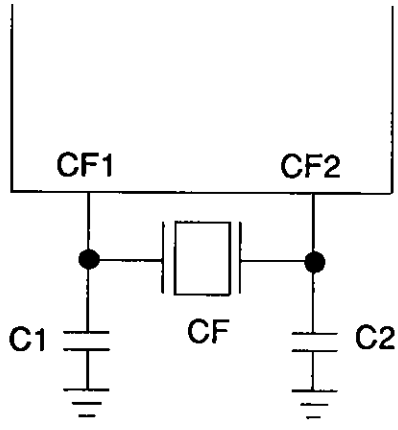


Figure 1 Main-clock circuit
Ceramic resonator oscillation

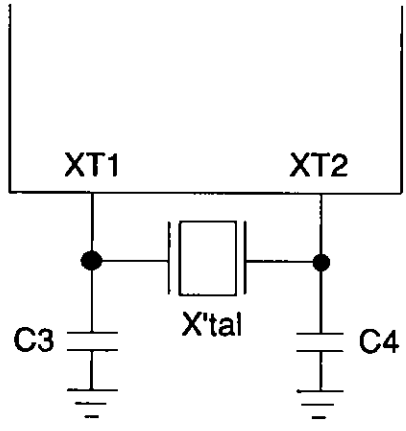


Figure 2 Sub-clock circuit
Crystal oscillation

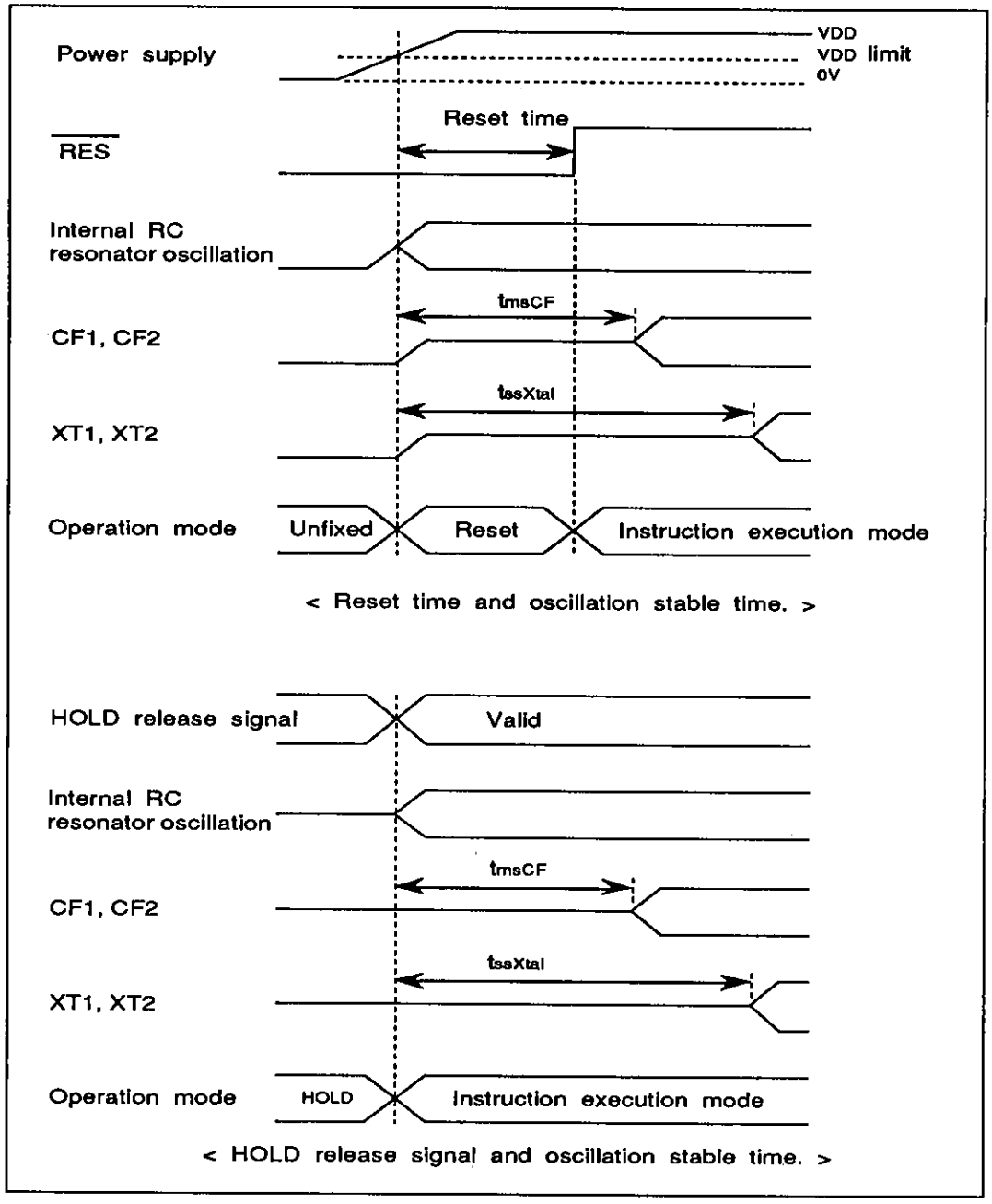
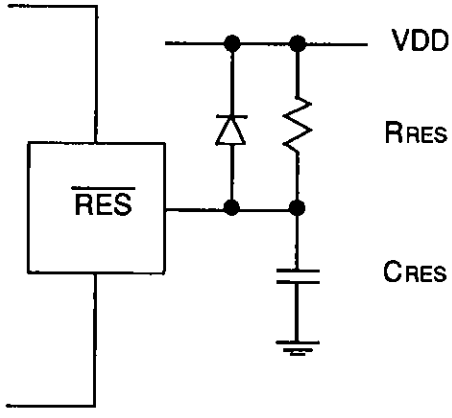
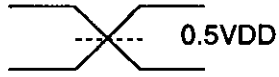


Figure 3 Oscillation stable time



(Note) Fix the value of CRES,RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit



< AC timing point >

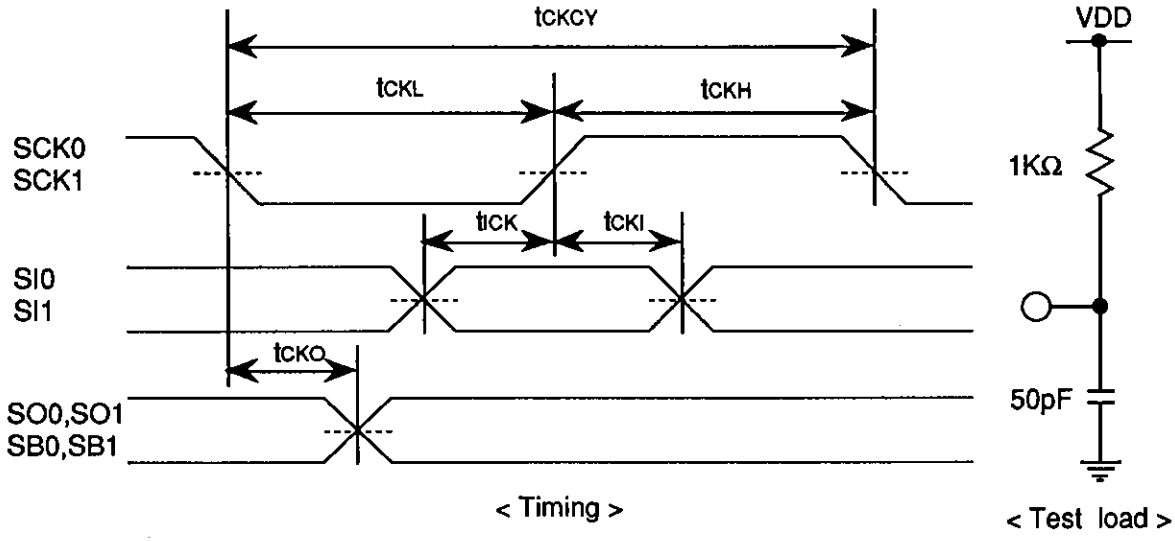


Figure 5 Serial input/outpu test condition

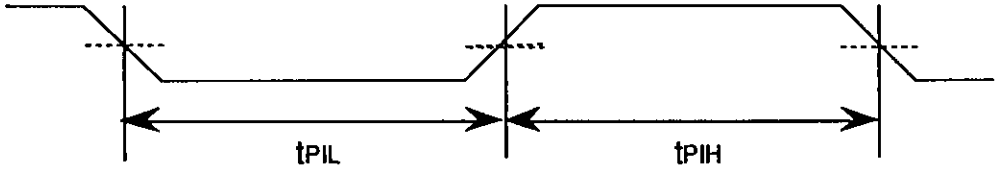


Figure 6 Pulse input timing condition